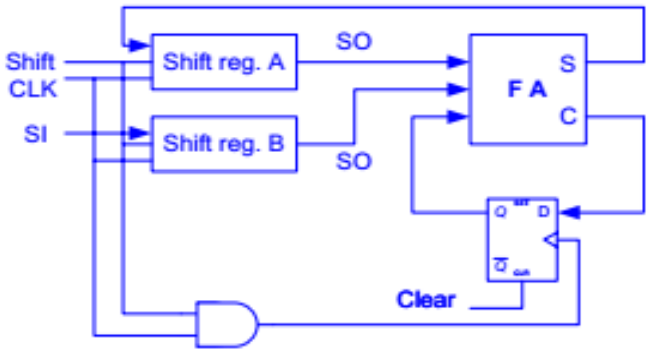
LECTURE 13: DIGITAL LOGIC CIRCUIT DESIGN

Serial Addition

We are going to investigate the operation of a serial adder in comparison to the parallel adder.

The two binary numbers to be added serially are stored in shift registers A and B. The carry of the full adder is stored in a D flip-flop and used as the carry-in with the next pair of bits to be added. The sum bit is shifted in shift register A to replace the first number. At the end of the number of clock pulses used to add the two numbers, the sum will be available in register A. Register B can be made to contain a third number to be added to the sum. This process can be repeated any number of times to add more than two numbers. The serial adder is shown in the following Figure.



Design of the Serial Adder

The serial adder can be designed using the design procedure of the clocked sequential circuits.

We wish to design a sequential circuit that can add two bits x and y provided by two shift registers together with a carry bit that can be obtained from the output Q of a storage element (flip-flop), and produces the sum bit that can be stored in a shift register and the carry bit that can be added to the next pair of bits.

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The number of inputs is n=2 → x and y

The number of outputs is m=1 → S

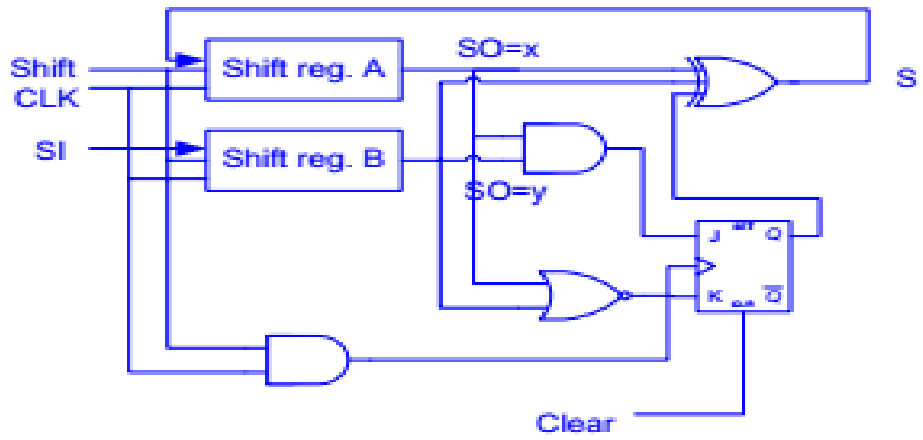
One flip-flop is needed to provide the carry-in for the addition. Let us choose a JK flip-flop. This description of the problem can be translated directly into a state table as follows:

P.S.	Inputs		N.S.	Output	Flip-Flop inputs	
Q	x	y	Q	S	J	K
0	0	0	0	0	0	X
0	0	1	0	1	0	X
0	1	0	0	1	0	X
0	1	1	1	0	1	X
1	0	0	0	1	X	1
1	0	1	1	0	X	0
1	1	0	1	0	X	0
1	1	1	1	1	X	0

The output and flip-flop input functions are then given by:

$$S = x \oplus y \oplus Q$$
$$J = xy \quad and \quad K = x'y' = (x + y)'$$

The circuit diagram consists of three gates and one flip-flop as shown in the following diagram.



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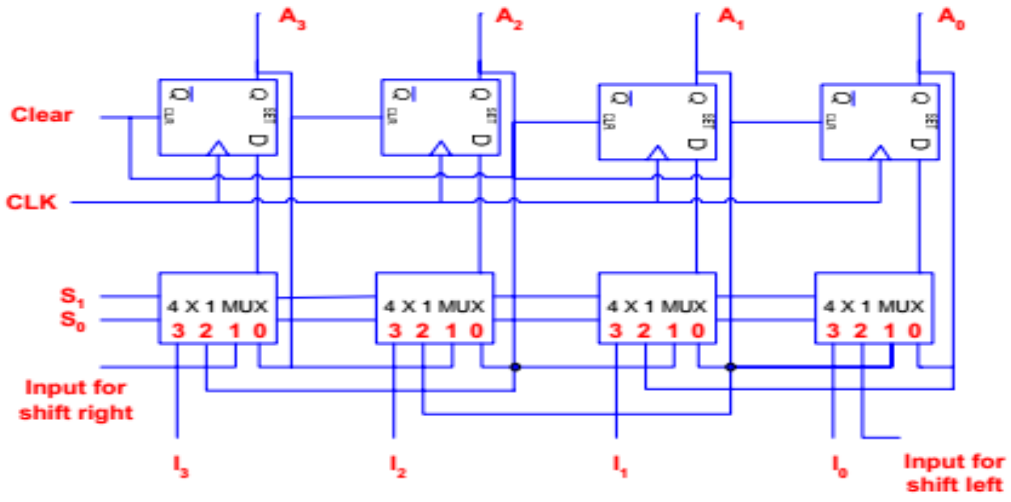
Universal Shift Register

Registers are available in integrated circuit form that can function as shift register in either direction (right or left), register with parallel load. Data can also be kept in the register while the clock pulses are applied. This universal register has the following capabilities:

1. **A clear (reset) input.**
2. **A clock input.**
3. **A shift right control.**
4. **A shift left control.**
5. **A parallel load control.**
6. **A control input to keep the contents of the register unchanged while clock pulses are applied.**

A universal shift register that has the previous capabilities is constructed using D flip flops and multiplexers. The construction of a 4-bit register is shown in the following diagram.



The function table for this register is given below.

Mode Control		
S_1	S_0	Operation
0	0	No change
0	1	Shift right
1	0	Shift left
1	1	Parallel load

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Ripple Counters

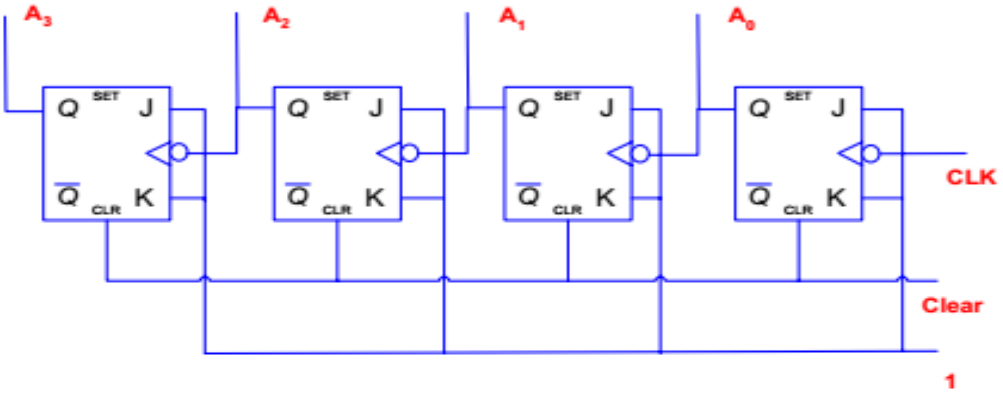
There are two categories of counters:

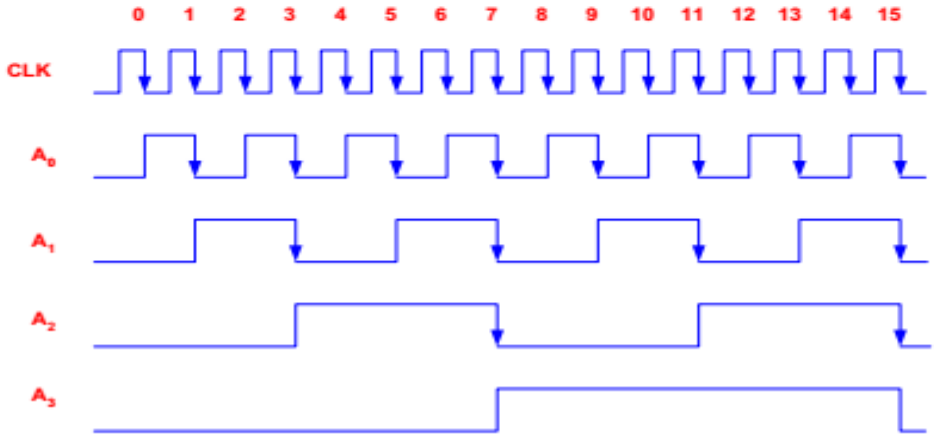
- Ripple counters,
- Synchronous counters.

Ripple counters are counters where each flip flop is triggered by the transition of other flip-flops. In synchronous counters all flip-flops are triggered by the same clock pulses.

Binary Ripple Counter

Binary ripple counter consists of a series of complementing flip-flops. A binary counter consisting of n flip-flops has a count cycle of 2^n and counts from 0 to 2^n-1. A 4-bit binary ripple counter using T flip-flops is shown.





Timing Diagram of the 4-bit ripple counter

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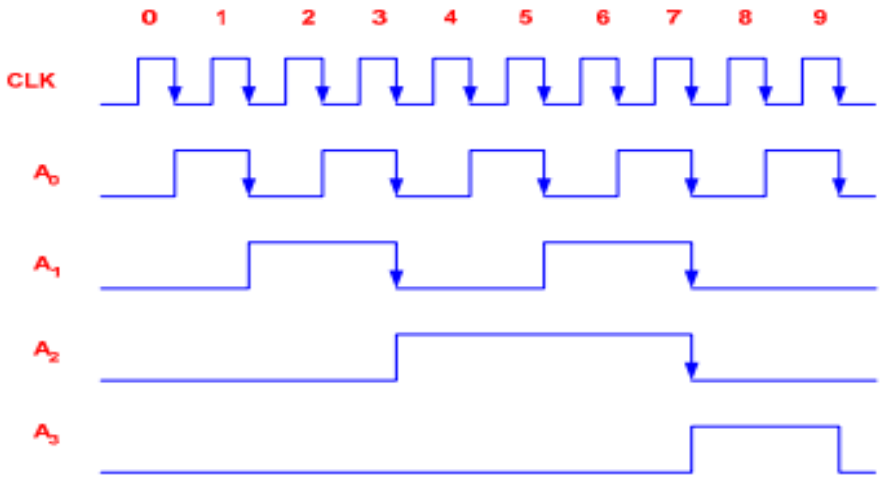
BCD Ripple Counter

The BCD ripple counter has a modulus of 10. It counts from 0 to 9 and then resets to 0. The timing diagram of this counter is shown. The main difference between this timing diagram and that of the binary counter is that A1 and A3 reset after the 10th pulse.



Timing Diagram of the BCD ripple counter

In order to arrive at the design of the BCD ripple counter, we must answer two questions concerning each flip-flop:

1. **Which source should trigger the flip-flop?**
2. **What values should we make the J and K inputs of the flip-flop?**

Using the timing diagram, it is clear that A_0 is to be triggered by the input clock pulses and the J and K inputs should be made 1 and 1. A_1 should be triggered by A_0. In order to prevent it from setting on the negative edge of pulse 9, we should make the J and

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K inputs equal to A_3' and 1. A_2 is triggered by A_1 and the J and K inputs are 1 and 1. Finally, A_3 should be triggered by A_0. TO

prevent A_3 from setting until we reach pulse 7, then we should make the J and K inputs equal to A_2A_1 and 1. The logic circuit of the BCD ripple counter is shown next.