# LECTURE 12: DIGITAL LOGIC CIRCUIT DESIGN

## Design Procedure

1. Derive a state diagram from the verbal description.
2. Reduce the number of states, if necessary.
3. Assign binary values to the states.
4. Obtain the state table.
5. Choose the type of flip-flops.
6. Derive the simplified flip-flop input equations and output equations.
7. Draw the logic diagram.

## Flip-Flop Excitation Tables

In the design of clocked sequential circuits, we know the present state and next state of the flip-flops. We need to find the flip-flop input functions and the output functions in order to design the combinational circuit part of the circuit. These functions can be easily obtained using the flip flop excitation table. These tables give us the required inputs that will achieve a given transition from $Q_t$ to $Q_{t+1}$.

The excitation table of the three types of flip-flops are:

D Flip-Flop Excitation Table

| $Q_t$ | $Q_{t+1}$ | D |
|---|---|---|
| 0 | 0 | 0 |
| 0 | 1 | 1 |
| 1 | 0 | 0 |
| 1 | 1 | 1 |

JK Flip-Flop Excitation Table

| $Q_t$ | $Q_{t+1}$ | J | K |
|---|---|---|---|
| 0 | 0 | 0 | X |
| 0 | 1 | 1 | X |
| 1 | 0 | X | 1 |
| 1 | 1 | X | 0 |

T Flip-Flop Excitation Table

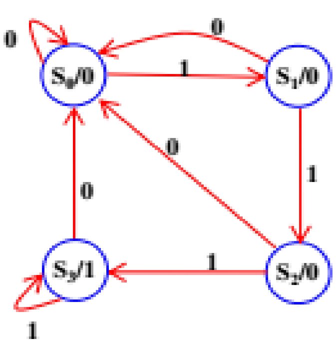
| $Q_t$ | $Q_{t+1}$ | T |
|---|---|---|
| 0 | 0 | 0 |
| 0 | 1 | 1 |
| 1 | 0 | 1 |
| 1 | 1 | 0 |

## Design of a Sequence Detector

We wish to design a circuit that detects three or more consecutive 1's in a string of bits coming through an input line. We start in the

initial state $S_0$. If the input is 0 then the circuit stays in $S_0$. the first input 1 will take the circuit to the next state $S_1$. Any input 0 will take the circuit back to state $S_0$. Only three consecutive 1's will take the circuit through the states $S_0$, $S_1$, $S_2$, and $S_3$. Any further 1's will leave the circuit in state $S_3$.

The state diagram is shown below



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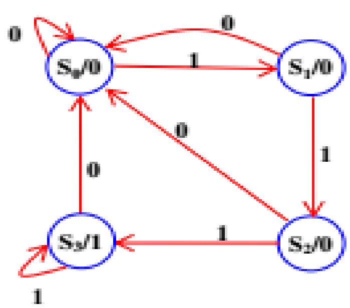
## Synthesis using D flip-flops

The state diagram is used to prepare the state table which is shown below.

| P.S. | | Input | N.S. | | Output |
|---|---|---|---|---|---|
| A | B | x | A | B | y |
| 0 | 0 | 0 | 0 | 0 | 0 |
| 0 | 0 | 1 | 0 | 1 | 0 |
| 0 | 1 | 0 | 0 | 0 | 0 |
| 0 | 1 | 1 | 1 | 0 | 0 |
| 1 | 0 | 0 | 0 | 0 | 0 |
| 1 | 0 | 1 | 1 | 1 | 0 |
| 1 | 1 | 0 | 0 | 0 | 1 |
| 1 | 1 | 1 | 1 | 1 | 1 |

## Design of a Sequence Detector using D Flip-Flops

The state diagram and the state table of the sequence detector are given below




| P.S. | | Input | N.S. | | Output |
|---|---|---|---|---|---|
| A | B | x | A | B | y |
| 0 | 0 | 0 | 0 | 0 | 0 |
| 0 | 0 | 1 | 0 | 1 | 0 |
| 0 | 1 | 0 | 0 | 0 | 0 |
| 0 | 1 | 1 | 1 | 0 | 0 |
| 1 | 0 | 0 | 0 | 0 | 0 |
| 1 | 0 | 1 | 1 | 1 | 0 |
| 1 | 1 | 0 | 0 | 0 | 1 |
| 1 | 1 | 1 | 1 | 1 | 1 |

We use two D flip-flops with the four states 00, 01, 10, and 11. The next state is equal to the flip-flop input. The state table may be considered as a truth table for the combinational circuit part.

The required functions are $D_A$, $D_B$, and the output y.

$$D_A(A,B,x) = \sum(3,5,7)$$

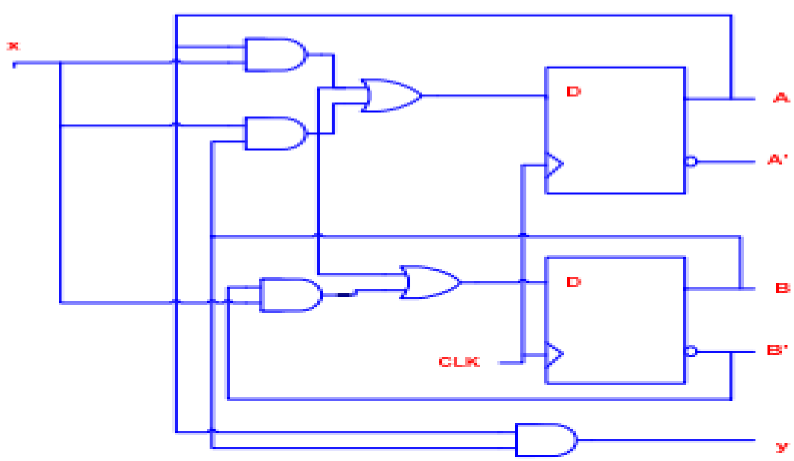
$$D_B(A,B,x) = \sum(1,5,7)$$

and $y(A,B,x) = \sum(6,7)$

These functions can be simplified and the logic circuit drawn.

$$D_A = Ax + Bx$$
$$D_B = Ax + B'x$$
$$y = AB$$

And the logic circuit is shown next.




## Design of Clocked Sequential Circuits Using JK Flip-Flops

When selecting the JK flip-flop in the design of clocked sequential circuits, we must use the excitation table of the flip-flop in order to obtain the flip-flop input functions. The following example illustrates the procedure:

### Example Of The Design Using JK Flip-Flops

Design the clocked sequential circuit that has the following state table using JK flip-flops.

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| P.S. | | Input | N.S. | |
|---|---|---|---|---|
| A | B | x | A | B |
| 0 | 0 | 0 | 0 | 0 |
| 0 | 0 | 1 | 0 | 1 |
| 0 | 1 | 0 | 1 | 0 |
| 0 | 1 | 1 | 0 | 1 |
| 1 | 0 | 0 | 1 | 0 |
| 1 | 0 | 1 | 1 | 1 |
| 1 | 1 | 0 | 1 | 1 |
| 1 | 1 | 1 | 0 | 0 |

We use the excitation table of the JK flip-flop in order to obtain the input functions of the flip-flops. The state table becomes the excitation table of the sequential circuit.

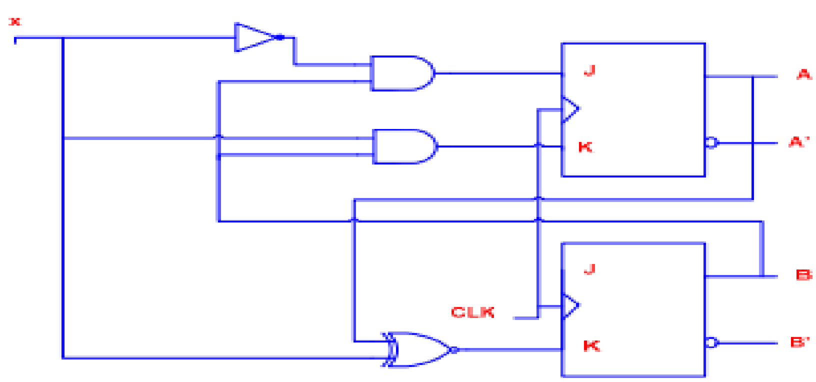
| P.S. | | Input | N.S. | | Flip-Flop Inputs | | | |
|---|---|---|---|---|---|---|---|---|
| A | B | x | A | B | $J_A$ | $K_A$ | $J_B$ | $K_B$ |
| 0 | 0 | 0 | 0 | 0 | 0 | X | 0 | X |
| 0 | 0 | 1 | 0 | 1 | 0 | X | 1 | X |
| 0 | 1 | 0 | 1 | 0 | 1 | X | X | 1 |
| 0 | 1 | 1 | 0 | 1 | 0 | X | X | 0 |
| 1 | 0 | 0 | 1 | 0 | X | 0 | 0 | X |
| 1 | 0 | 1 | 1 | 1 | X | 0 | 1 | X |
| 1 | 1 | 0 | 1 | 1 | X | 0 | X | 0 |
| 1 | 1 | 1 | 0 | 0 | X | 1 | X | 1 |

The excitation table can now be treated as a truth table for the combinational circuit part. We can obtain the Boolean expressions of the required functions and simplify them using Karnaugh maps.

$J_A = Bx'$ $\qquad$ $K_A = Bx$

$J_B = x$ $\qquad$ and $\qquad$ $K_B = A'x' + Ax = (A \oplus x)'$

The logic circuit can then be drawn.

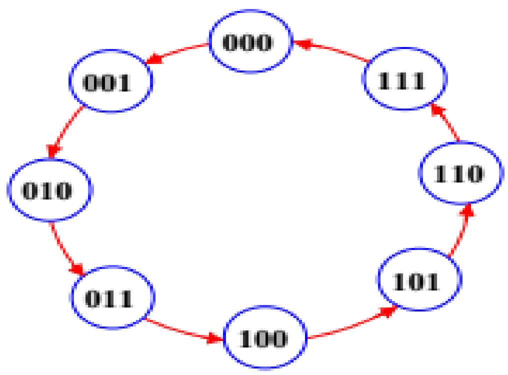


## Design of a Binary Counter Using T Flip-Flops

We are going to design a binary counter as an example for the synthesis procedure using T flip-flops.

A binary counter of n flip-flops will be able to count from 0 to a maximum count of 2n-1. As an example a binary counter comprising three flip-flops will count from 000 to 111 and then resets to 000. We wish to design such counter using T flip-flops.

The state diagram of such counter is shown.



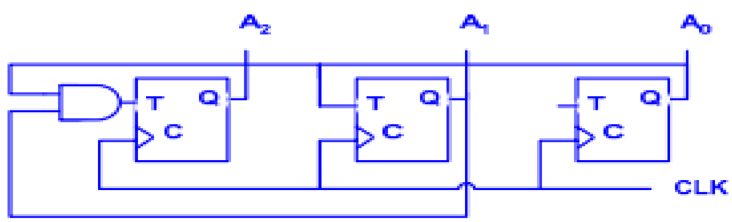

The excitation table of the circuit, which is shown next, consists of the state table together with the flip-flop input functions which can be completed with the aid of the T flip-flop excitation table.

| P.S. | | | N.S. | | | Flip-Flop Inputs | | |
|---|---|---|---|---|---|---|---|---|
| $A_2$ | $A_1$ | $A_0$ | $A_2$ | $A_1$ | $A_0$ | $T_{A2}$ | $T_{A1}$ | $T_{A0}$ |
| 0 | 0 | 0 | 0 | 0 | 1 | 0 | 0 | 1 |
| 0 | 0 | 1 | 0 | 1 | 0 | 0 | 1 | 1 |
| 0 | 1 | 0 | 0 | 1 | 1 | 0 | 0 | 1 |
| 0 | 1 | 1 | 1 | 0 | 0 | 1 | 1 | 1 |
| 1 | 0 | 0 | 1 | 0 | 1 | 0 | 0 | 1 |
| 1 | 0 | 1 | 1 | 1 | 0 | 0 | 1 | 1 |
| 1 | 1 | 0 | 1 | 1 | 1 | 0 | 0 | 1 |
| 1 | 1 | 1 | 0 | 0 | 0 | 1 | 1 | 1 |

From the table, and using Karnaugh maps for simplifications, we get:

$T_{A2} = A_1 A_0$ $T_{A1} = A_0$ and $T_{A0} = 1$

The logic diagram is shown.

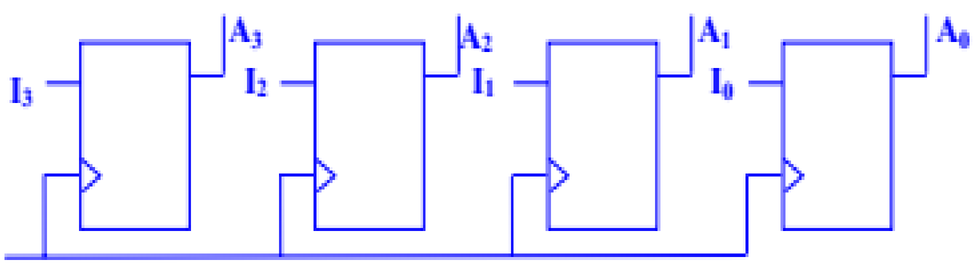



## Introduction to Registers and Counters

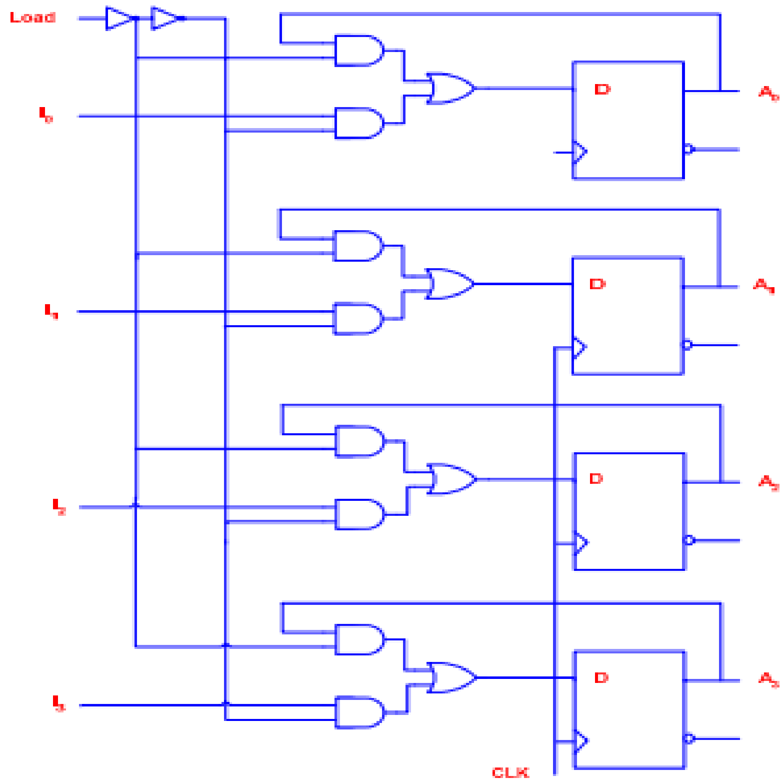
Registers and counters are practical examples of clocked sequential circuits. A register consists of a group of flip-flops each is capable of storing one bit of information. Logic gates could be used to arrange the loading of the register with data and reading of the contents. Counters may be considered as a special register, which counts in a certain count cycle determined by the design of the counting register.

## A Simple 4-Bit Register

The following diagram shows a 4-bit register consisting of D flip-flops.



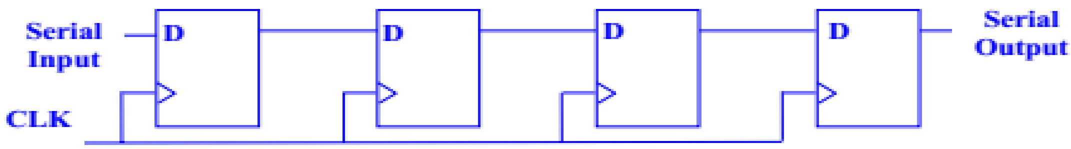
## 4-Bit Register with Parallel Load




The next state of the D flip-flop is equal to the D input. In order to keep the contents of the register unchanged while the clock pulses are applied, then the output is applied back to the D input when the load input is zero. When we want to load the register with new input I, then the load input goes to one, then D=I.

## Shift Registers

Shift registers are registers that can shift binary bits in one direction or both directions upon the application of clock pulses. A 4-bit shift register is shown next. This is a shift right shift register as seen by the position of the serial input and serial output.

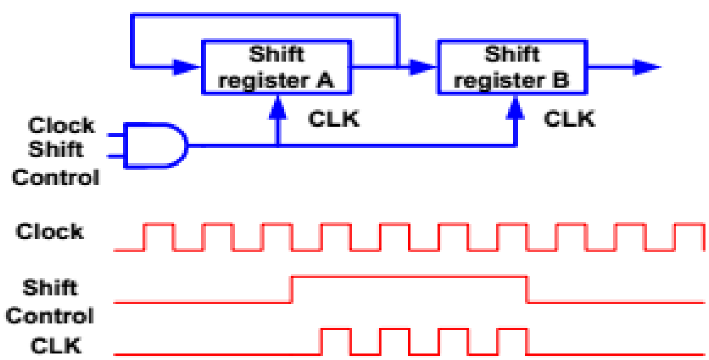



## Serial Transfer

Serial transfer means that data is manipulated or transferred in the digital system one bit at a time. In the other method of transfer, which is called parallel transfer, data is transferred at the same time (by means of one clock pulse).

In the following Figure, data is transferred from register A to register B upon the application of four clock pulses. At the same time the 4 bits remain in register A by circulating it back in the register.

The contents of registers A and B before and after the application of the four clock pulses are given in the table.




If register A contains 1100 and register B 0101 initially. The contents of registers A and b after each clock pulse are given in the following table.

| Timing pulse | Shift register A | | | | Shift register B | | | |
|---|---|---|---|---|---|---|---|---|
| Initial | 1 | 1 | 0 | 0 | 0 | 1 | 0 | 1 |
| After T1 | 0 | 1 | 1 | 0 | 0 | 0 | 1 | 0 |
| After T2 | 0 | 0 | 1 | 1 | 0 | 0 | 0 | 1 |
| After T3 | 1 | 0 | 0 | 1 | 1 | 0 | 0 | 0 |
| After T4 | 1 | 1 | 0 | 0 | 1 | 1 | 0 | 0 |