Hardware architecture of 8086 and 8088 Microprocessors

Objective:

- To examine the 8086 and 8088 microprocessors in terms of hardware point of view

- To introduce the operating modes and functions of signals Generated/accepted by 8086 and 8088 microprocessors

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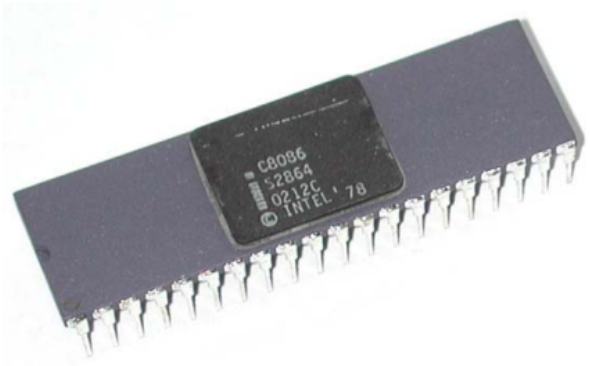
Slide 1: **The hardware architecture of 8086 and 8088 processors:**

- The microprocessors 8086 and 8088 were both made of **HMOS** technology with an IC circuitry equivalent to ≈ 29000 transistors. (*HMOS: high performance metal oxide semiconductor*)

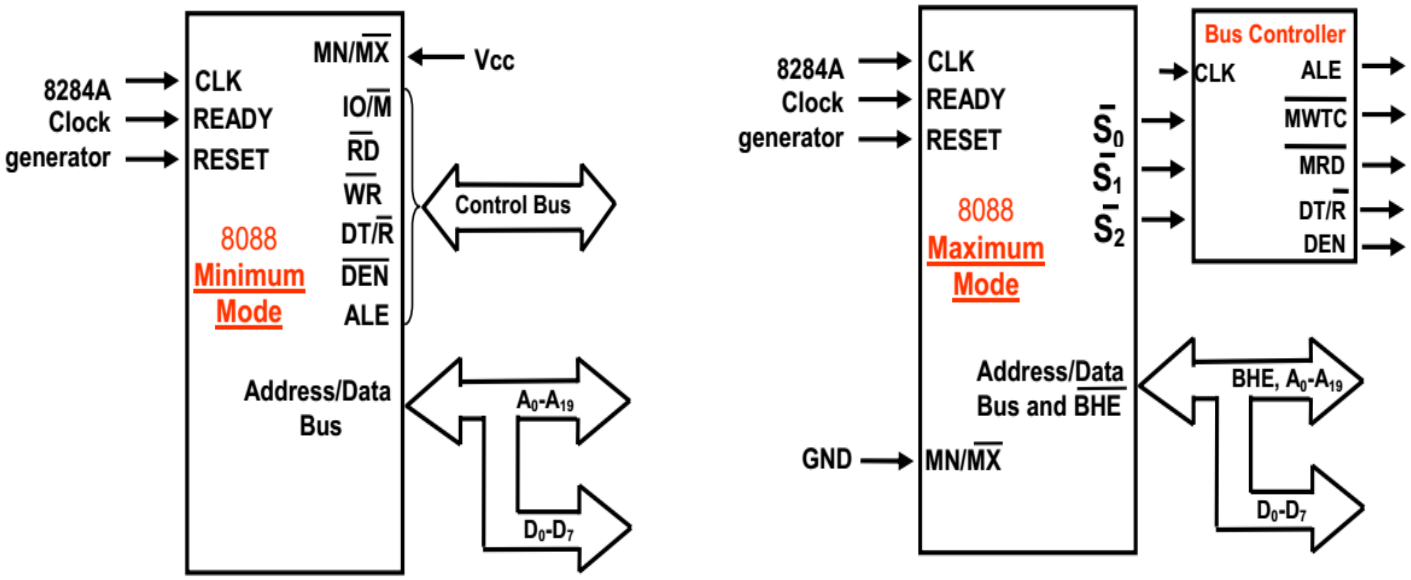
- Unlike the software model, the hardware architecture of 8088 microprocessor is different from that of 8086 (Talk only: ***As 8086 has 16-bit data bus and 8088 has 8-bit data bus as will be demonstrate in Slides 4 and 5)***

- Both processors are housed in a 40-pin dual in-line package, with many of the pins having multiple fictions or Multiplexed.



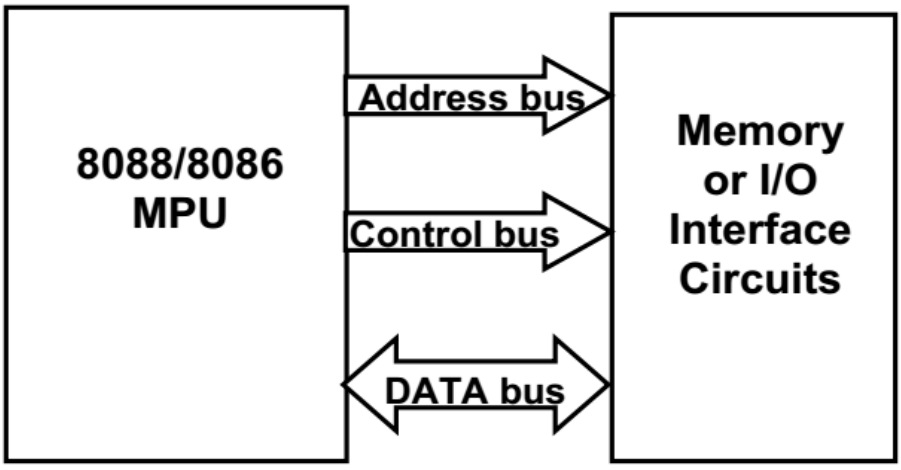
Slide 2: **The Modes of Operation:**

- The microprocessors 8086 and 8088 can be configured to work in two modes: The Minimum mode and the Maximum mode.
- The Minimum mode is used for single processor system, where 8086/8088 directly generates all the necessary control signals.
- The Maximum mode is designed for multiprocessor systems, where an additional "Bus-controller" IC is required to generate the control signals. The processors control the Bus-controller using status-codes.

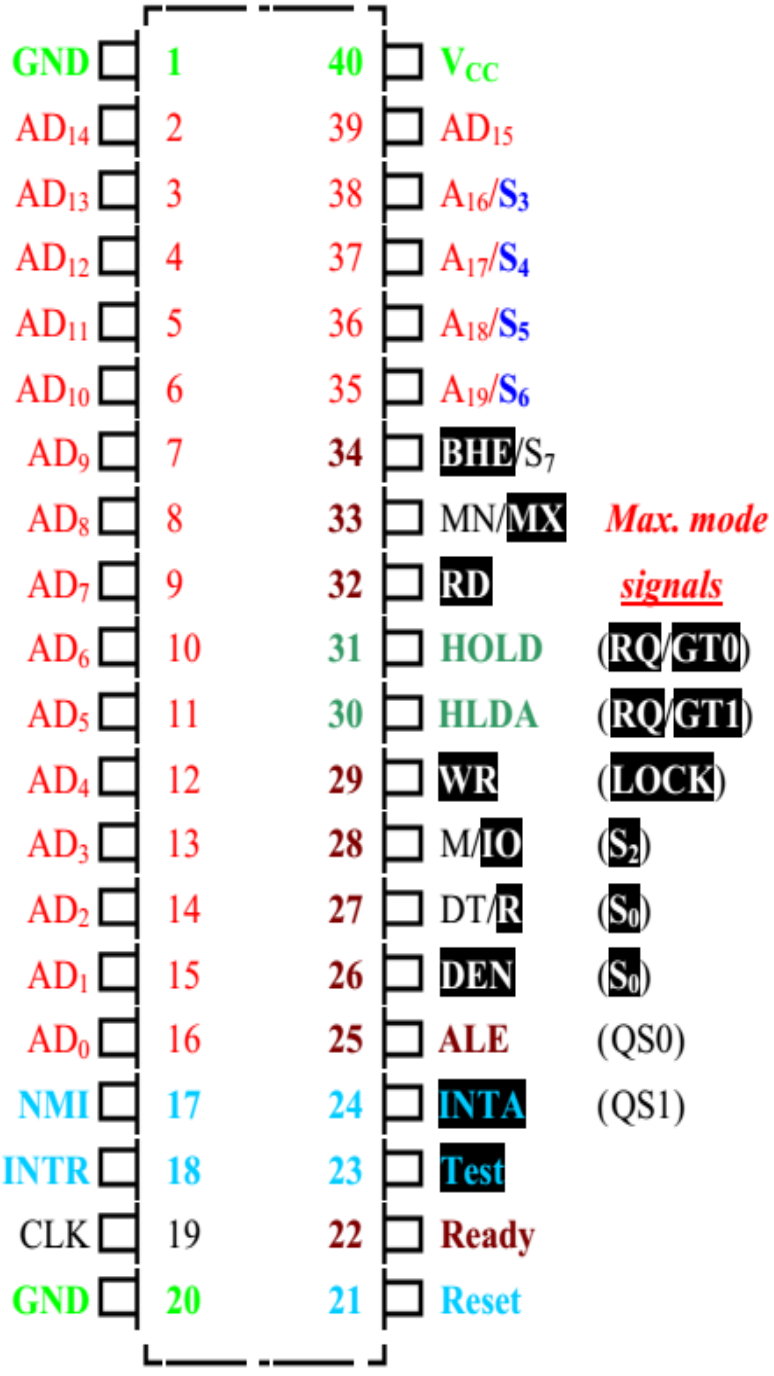


Slide 3: **Bus structure of 8086 based computer system:**

- A set of conductors, used for communicating information between the components in a computer system is called System-Bus.
    - Internal Bus: connects two minor components within a major component (or IC), such the connection between the control unit and internal registers of the MPU)
    - External Bus: connects two major components, such as MPU and an interface (Memory or input/output). Although some systems include more than one external bus, 8086 and 8088 processors contain one bus called system-bus.
- Typical system-bus includes; Address-bus (*carries physical address of memory storages or input/output locations*), Data-bus (*carries data to be read or written into MPU registers*) and Control-bus(*carries information to control the read or write operation*).
- In addition to CPU, the bus-system is also used by other components of the computer, during which the address, data and control pins of the CPU remains logically disconnected or at high-impedance state.



Slide 4: **The Pin-configuration of 8086 Microprocessor IC:**



Note that signals can be divided into following groups:

Address & Data signals:
- Address BUS (A_0-A_{19})
- Data BUS (D_0-D_7 & D_0-D_{15})
  (Note, **Multiplexed** pins)

Control Signals:
- MN/$\overline{MX}$ signal
- ALE signal
- $(IO/\overline{M})_{8088}$
- $\overline{RD}$ and $\overline{WT}$ signals
- DT/$\overline{R}$ signal
- $\overline{DEN}$ signal (*Min.* ≠ *Max.*)
- $\overline{SSO}$ signal etc……..

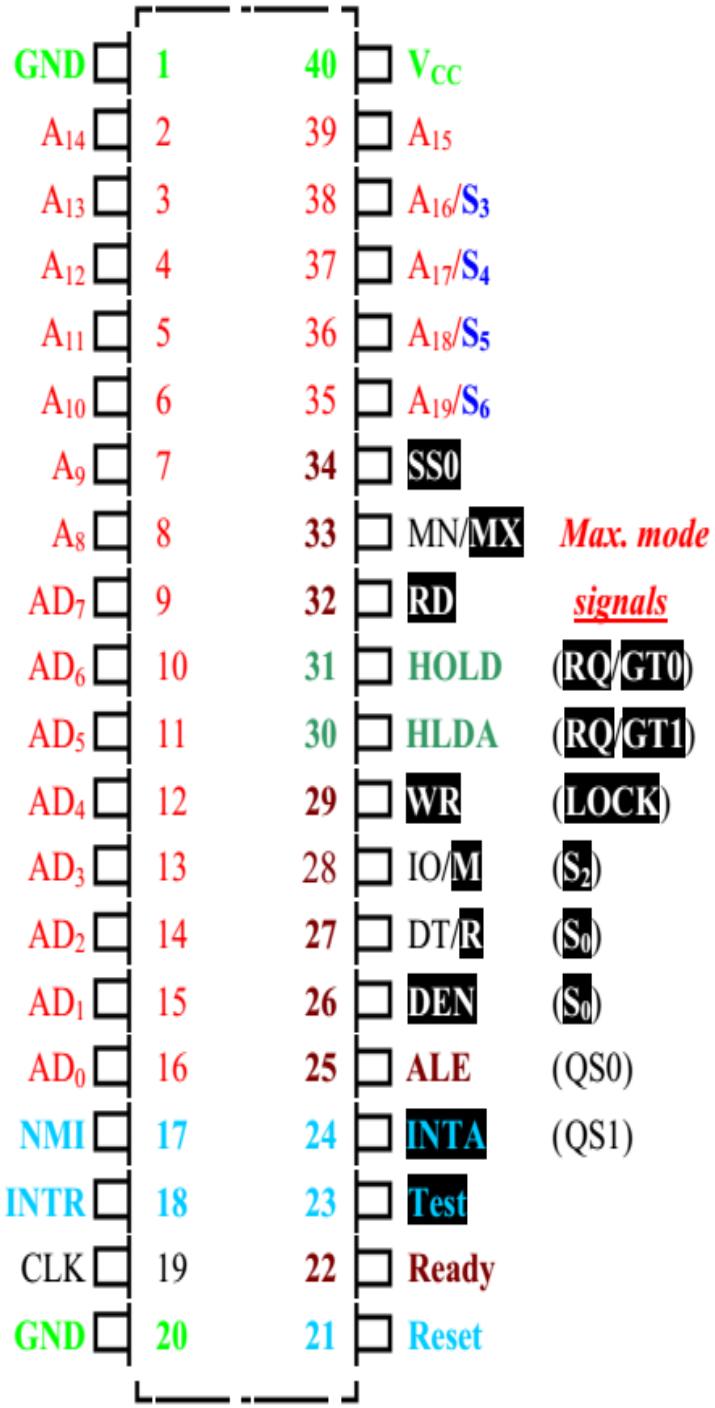
Status Signals:
- S_3 to S_6 signals
  (multiplex with address pins)

Interrupt Signals:
- INTR and $\overline{INTA}$ signals
- $\overline{TEST}$ signal

DMA interface Signals:
- **HOLD/HLDA**

Detail description of this signals are given in the following slides.

Slide 5: The Pin-configuration of 8088 Microprocessor IC:



- Some of the differences between the hardware configuration of 8086 and 8088 microprocessors are :

(a) 8086 uses 16-bit Data-bus (AD_0-AD_{16}) and 8088 uses 8-bit Data-bus (AD_0-AD_7)

(b) Pin 34 and 28 generates different signals in these microprocessors, as will be explained in later slides

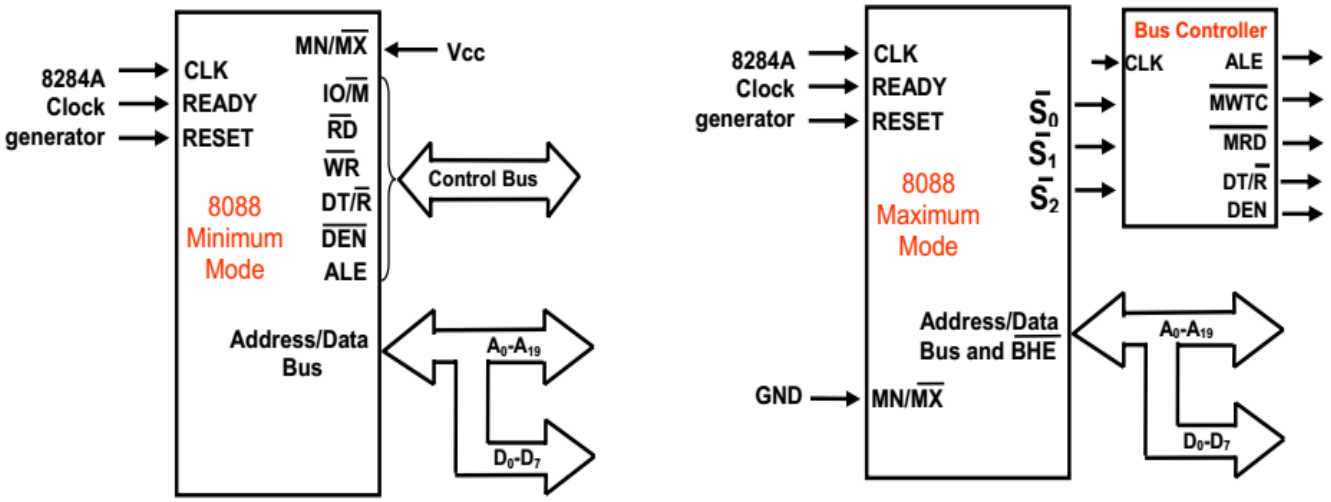
The differences between minimum mode and maximum mode operation of CPU are clear from the different signals of pin 24 to 31

Slide 6: **Definition of signals from 8086/8088 IC pin's :**

- Pins 2 to 16 and pins 35 to 39 of 8086/8088 IC generate address signals (A_{19}-A_0). This 20-bit **address bus** allows the processor to access 1 Mega, Byte-wide, memory storage locations or 64 kilo, byte-wide, input/output ports.

- In 8086 IC, Pin 2 to 16 and pin 39 generates/receives 16-bit data signals (D_{15}-D_0) to write/read data into the CPU registers. Thus, **Data bus** supports bi-directional data flow. But in 8088 IC, the Data bus is 8-bit wide and consists of data signals from Pin's 9 to 16.

- Note: Address-bus and Data-Bus in both 8088 and 8086 uses *Multiplexed pins*.



Slide 7: **Definition of signals from 8086/8088 IC pin's (cont'd) :**

- Pin 33 of 8088 and 8086 IC accepts *Minimum and Maximum mode* (MN/$\overline{MX}$) signal to select the processors operating mode. Thus, MN/$\overline{MX}$='1' initiates minimum mode and MN/$\overline{MX}$='0' initiates maximum mode of operation.

- Pin 28 outputs *Memory/Input-Output* signal of $(M/\overline{IO})_{for\ 8086}$ and $(IO/M)_{for\ 8088}$ to control the interfaces between the CPU, input-output and memory devices. Thus, for ***8088***, *IO/M='0' will interface the CPU with Memory storage locations and IO/M='1' will interface the CPU input/output ports.*

- Pin 25 controls *Address Latch Enable* (ALE) signal (pulse) to indicate that valid physical-address is present in the address-bus (A_{19}-A_0). During this pulsed period, address/data-multiplexed-pins carries Address-information to locate desired I/O or memory location.

Slide 8: **Definition of signals from 8086/8088 IC pin's (cont'd) :**

- In minimum mode, Pin 32 outputs *Read* ($\overline{RD}$) signal to control the data reading process of the microprocessor. Thus, $\overline{RD}$='0' initiates the data read operation and continues until $\overline{RD}$='1'.

But in maximum mode, appropriate status codes ($\overline{S_2}$, $\overline{S_1}$, $\overline{S_0}$) are outputted by pins 26 to 28 to generate a *Memory ReaD Command* ($\overline{MRDC}$) signal from the bus controller IC. Thus, for $\overline{S_2}$=1, $\overline{S_1}$=0, $\overline{S_0}$=1 the bus-controller IC outputs $\overline{MRDC}$='0' to initiate maximum mode memory read operation (*talk only: review both figures to better understand the operation of this control signal*)

Slide 9: **Definition of signals from 8086/8088 IC pin's (cont'd) :**

- In minimum mode, Pin 29 outputs *Write* ($\overline{WR}$) signal to control the writing process of the microprocessor. Thus, to initiate and maintain the writing process, CPU needs to output $\overline{WT}$='0' and $\overline{RD}$='1' signals

But in maximum mode, the appropriate status code ($\overline{S_2}$, $\overline{S_1}$, $\overline{S_0}$) is outputted from pins 26 to 28, which in return generates *Memory WriTe Command* (MWTC) or Advance Memory *Write* Command ($\overline{AMWC}$) signals to initiate memory write operation.

- Pin 27 outputs *Data transmit/receive* ($DT/\overline{R}$) signal to control the direction of data transfer mode (receive/transmit) in the 'Data-Bus-

Transceiver-buffer IC'. Thus for ***8088***, *if DT/R='0', transceiver buffer IC will be programmed to support Data-receive (or read) operation.*

Slide 10: **Definition of signals from 8086/8088 IC pin's (cont'd) :**

- In minimum mode, Pin 26 outputs *Data Enable* ($\overline{DEN}$='0') signal to control the Data-bus-transceiver-buffer IC. But in maximum mode, appropriate status code ($\overline{S_2}$, $\overline{S_1}$, $\overline{S_0}$) from pins 26 to 28 of the microprocessor enables the Bus-controller IC to generate (DEN='1') signal, which activates the transceiver-buffer IC.

- In 8088, Pin 34 outputs *Status line* ($\overline{SSO}$) signal to indicate if code or data is accessed during the ongoing bus-cycle. Thus, $\overline{SSO}$='0' means code is being read or written.

But in 8086 mode, Pin 34 outputs Bank-*high-enable* ($\overline{BHE}$) signal to control the access of High (even) or Low (odd) main memory banks.

- In both MPU's, pin 22 accepts READY signal from external circuits to prolong the BUS-Cycle, by inserting wait-status if and when required. This enhances the compatibility between high-speed CPU with relatively slower peripheral devices.

Slide 11: **Definition of signals from 8086/8088 IC pin's (cont'd) :**

- In maximum mode, pin 29 outputs $\overline{\text{LOCK}}$ signal, which in a multiprocessor system locks other processors off the system-bus during its interaction with common system resources via that system-bus.

- In Minimum mode, external device sends HOLD interrupt signal to pin 31of the processor to indicate its necessity to take control of the system-bus. In response, the processor completes the job at hand and outputs HLDA (hold acknowledged signal) interrupt signal via pin 30, which indicates to the external device that it can take control the system bus. During this process, most of the address, data, control pins of the CPU remain in **high-Z** state.

- To perform system reset, external interrupt signal is inputted into the processor via Pin 22. This interrupt signal initiates hardware reset and initialize CPU-registers,