

Control Word Format of 8255

Mode 1: (Strobed input/output mode) In this mode the handshaking control the input and output action of the specified port. Port C lines PC0-PC2, provide strobe or handshake lines for port B. This group which includes port B and PC0-PC2 is called as group B for Strobed data input/output. Port C lines PC3-PC5 provide strobe lines for port A. This group including port A and PC3-PC5 from group A. Thus port C is utilized for generating handshake signals. The salient features of mode 1 are listed as follows:

1. Two groups – group A and group B are available for strobed data transfer.
 2. Each group contains one 8-bit data I/O port and one 4-bit control/data port.
 3. The 8-bit data port can be either used as input and output port. The inputs and outputs both are latched.
 4. Out of 8-bit port C, PC0-PC2 are used to generate control signals for port B and PC3-PC5 are used to generate control signals for port A. the lines PC6, PC7 may be used as independent data lines.
- **The control signals for both the groups in input and output modes are explained as follows:**

Input control signal definitions (mode 1):

- **STB** (Strobe input) – If this lines falls to logic low level, the data available at 8-bit input port is loaded into input latches.
- **IBF** (Input buffer full) – If this signal rises to logic 1, it indicates that data has been loaded into latches, i.e. it works as an acknowledgement. IBF is set by a low on STB and is reset by the rising edge of RD input.
- **INTR** (Interrupt request) – This active high output signal can be used to interrupt the CPU whenever an input device requests the service. INTR is set by a high.STB pin and a high at IBF pin. INTE is an internal flag that can be controlled by the bit set/reset mode of either PC4(INTEA) or PC2(INTEB) as shown in fig.
- INTR is reset by a falling edge of RD input. Thus an external input device can be request the service of the processor by putting the data on the bus and sending the strobe signal.

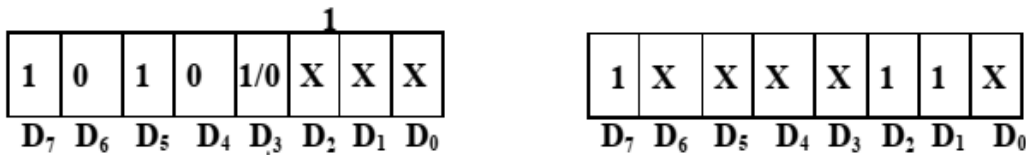
Output control signal definitions (mode 1) :

- **OBF** (Output buffer full) – This status signal, whenever falls to low, indicates that CPU has written data to the specified output port. The OBF flip-flop will be set by a rising edge of WR signal and reset by a low going edge at the ACK input.
- **ACK** (Acknowledge input) – ACK signal acts as an

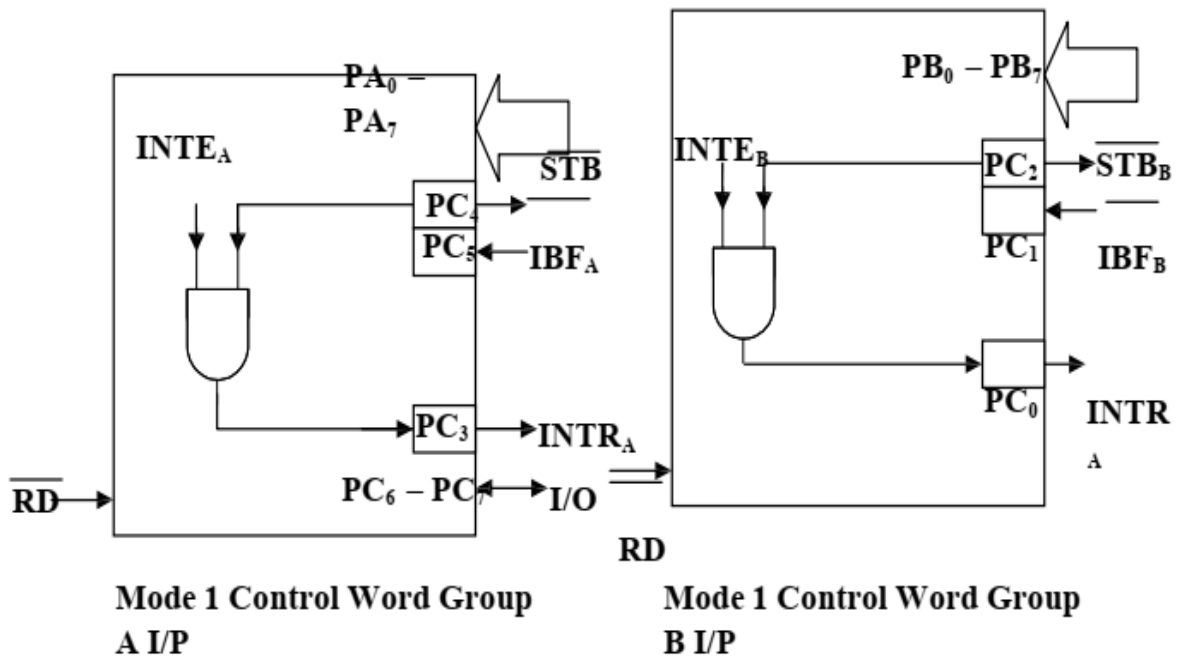
acknowledgement to be given by an output device. ACK signal, whenever low, informs the CPU that the data transferred by the CPU to the output device through the port is received by the output device.

- **INTR** (Interrupt request) – Thus an output signal that can be used to interrupt the CPU when an output device acknowledges the data received from the CPU. INTR is set when ACK, OBF and INTE are 1. It is reset by a falling edge on WR input. The INTEA and INTEB flags are controlled by the bit set-reset mode of PC6 and PC2 respectively.

Input control signal definitions in Mode 1



1 - Input
0 - Output
For PC₆ - PC₇



Programmable Interval Timer 8253

- The Intel 8253 is a programmable counter / timer chip designed for use as an Intel microcomputer peripheral. It uses nMOS technology with a single +5V supply and is packaged in a 24-pin plastic DIP.
- It is organized as 3 independent 16-bit counters, each with a counter rate up to 2 MHz. All modes of operation are software programmable.
- The 82C54 is pin compatible with the HMOS 8254, and is a superset of the 8253.
- Six programmable timer modes allow the 82C54 / 8253 to be used as an event counter, elapsed time indicator, programmable one-shot, and in many other applications.

Block diagram

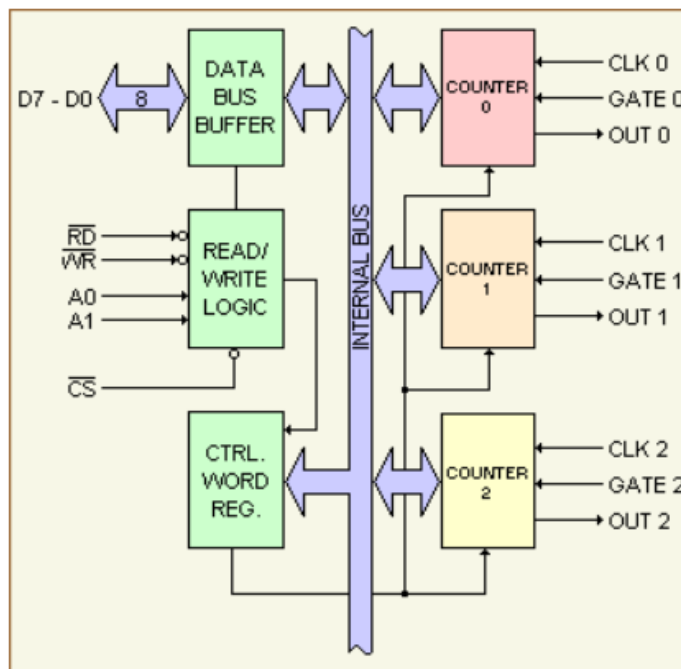


Fig: Block diagram of an 8253 programmable interval timer

The block labeled *data bus buffer* contains the logic to buffer the data bus to / from the microprocessor, and to the internal registers. The block labeled *read / write logic* controls the reading and the writing of the counter registers. The final block, the *control word register*, contains the programmed information that is sent to the device from the microprocessor. In effect this register defines how the 8253 logically works. The timer has three independent, programmable counters and they are all identical

Each counter in the block diagram has 3 logical lines connected to it. Two of these lines, clock and gate, are inputs. The third, labeled OUT is an output. The function of these lines changes and depends on how the device is initialized or programmed.