# PIO 8255

- The parallel input-output port chip 8255 is also called as programmable ***peripheral input-output port.*** The Intel's 8255 is designed for use with Intel's 8- bit, 16-bit and higher capability microprocessors. It has 24 input/output lines which may be individually programmed in two groups of twelve lines each, or three groups of eight lines.
- The two groups of I/O pins are named as Group A and Group B. Each of these two groups contains a subgroup of eight I/O lines called as 8-bit port and another subgroup of four lines or a 4-bit port. Thus Group A contains an 8-bit port A along with a 4-bit port C upper.
- The port A lines are identified by symbols $PA_0$-$PA_7$ while the port C lines are identified as $PC_4$-$PC_7$. Similarly, Group B contains an 8-bit port B, containing lines PB0-PB7 and a 4-bit port C with lower bits PC0- PC3. The port C upper and port C lower can be used in combination as an 8-bit port C.
- Both the port C are assigned the same address. Thus one may have either three 8- bit I/O ports or two 8-bit and two 4-bit ports from 8255. All of these ports can

  function independently either as input or as output ports. This can be achieved by programming the bits of an internal register of 8255 called as control word register (CWR).
- The internal block diagram and the pin configuration of 8255 are shown in fig.
- The 8-bit data bus buffer is controlled by the read/write control logic. The read/write control logic manages all of the internal and external transfers of both data and control words.
- $\overline{RD}$ , $\overline{WR}$ , $A_1$, $A_0$ and RESET are the inputs provided by the microprocessor to the READ/ WRITE control logic of 8255. The 8-bit, 3-state bidirectional buffer is used to interface the 8255 internal data bus with the external system data bus.
- This buffer receives or transmits data upon the execution of input or output instructions by the microprocessor. The control words or status information is also transferred through the buffer.
- The signal description of 8255 are briefly presented as follows :
- **$PA_7$-$PA_0$**: These are eight port A lines that acts as either latched output or buffered input lines depending upon the control word loaded into the control word register.
- **$PC_7$-$PC_4$** : Upper nibble of port C lines. They may act as either output latches or input buffers lines.This port also can be used for generation of handshake lines in mode 1 or mode 2.
- **$PC_3$-$PC_0$** : These are the lower port C lines, other details are the same as PC7-PC4 lines.

- **$PB_0$-$PB_7$** : These are the eight port B lines which are used as latched output lines or buffered input lines in the same way as port A.
- **$\overline{RD}$** : This is the input line driven by the microprocessor and should be low to indicate read operation to 8255.
- **$\overline{WR}$** : This is an input line driven by the microprocessor. A low on this line indicates write operation.
- **$\overline{CS}$** : This is a chip select line. If this line goes low, it enables the 8255 to respond to RD and WR signals, otherwise RD and WR signal are neglected.
- **$A_1$-$A_0$** : These are the address input lines and are driven by the microprocessor.

  These lines $A_1$-$A_0$ with $\overline{RD}$, $\overline{WR}$ and CS from the following operations for 8255. These address lines are used for addressing any one of the four registers, i.e.three ports and a control word register as given in table below.
- In case of 8086 systems, if the 8255 is to be interfaced with lower order data bus, the $A_0$ and $A_1$ pins of 8255 are connected with $A_1$ and $A_2$ respectively.
- **$D_0$-$D_7$** : These are the data bus lines those carry data or control word to/from the microprocessor.
- **RESET** : A logic high on this line clears the control word register of 8255. All ports are set as input ports by default after reset.

| $\overline{RD}$ | $\overline{WR}$ | $\overline{CS}$ | $A_1$ | $A_0$ | Input (Read) cycle |
|---|---|---|---|---|---|
| 0 | 1 | 0 | 0 | 0 | Port A to Data bus |
| 0 | 1 | 0 | 0 | 1 | Port B to Data bus |
| 0 | 1 | 0 | 1 | 0 | Port C to Data bus |
| 0 | 1 | 0 | 1 | 1 | CWR to Data bus |

| $\overline{RD}$ | $\overline{WR}$ | $\overline{CS}$ | $A_1$ | $A_0$ | Output (Write) cycle |
|---|---|---|---|---|---|
| 1 | 0 | 0 | 0 | 0 | Data bus to Port A |
| 1 | 0 | 0 | 0 | 1 | Data bus to Port B |
| 1 | 0 | 0 | 1 | 0 | Data bus to Port C |
| 1 | 0 | 0 | 1 | 1 | Data bus to CWR |

| $\overline{RD}$ | $\overline{WR}$ | $\overline{CS}$ | $A_1$ | $A_0$ | Function |
|---|---|---|---|---|---|
| X | X | 1 | X | X | Data bus tristated |
| 1 | 1 | 0 | X | X | Data bus tristated |

# Control Word Register

# Block Diagram of 8255 (Architecture)

- It has a 40 pins of 4 groups.

1. Data bus buffer
2. Read Write control logic
3. Group A and Group B controls
4. Port A, B and C

- ***Data bus buffer***: This is a tristate bidirectional buffer used to interface the 8255 to system databus. Data is transmitted or received by the buffer on execution of
  input or output instruction by the CPU.
- Control word and status information are also transferred through this unit.
- ***Read/Write control logic***: This unit accepts control signals ( $\overline{RD}$ , $\overline{WR}$ ) and also inputs from address bus and issues commands to individual group of control blocks (Group A, Group B).
- It has the following pins.

a) $\overline{CS}$ – Chipselect : A low on this PIN enables the communication between CPU and 8255.

b) $\overline{RD}$ (Read) – A low on this pin enables the CPU to read the data in the ports or the status word through data bus buffer.

c) $\overline{WR}$ (Write) : A low on this pin, the CPU can write data on to the ports or on to the control register through the data bus buffer.

d) **RESET**: A high on this pin clears the control register and all ports are set to the input mode.

e) **A0** and **A1** (Address pins): These pins in conjunction with $\overline{RD}$ and $\overline{WR}$ pins control the selection of one of the 3 ports.

- ***Group A and Group B controls*** : These block receive control from the CPU and issues commands to their respective ports.
- Group A - PA and PCU (PC7 –PC4)
- Group B - PCL (PC3 – PC0)
- Control word register can only be written into no read operation of the CW register is allowed.
- a) **Port A**: This has an 8 bit latched/buffered O/P and 8 bit input latch. It can be programmed in 3 modes – mode 0, mode 1, mode 2.

b) **Port B**: This has an 8 bit latched / buffered O/P and 8 bit input latch. It can be programmed in mode 0, mode1.

c) **Port C** : This has an 8 bit latched input buffer and 8 bit output latched/buffer. This port can be divided into two 4 bit ports and can be used as control signals for port A and port B. it can be programmed in mode 0.

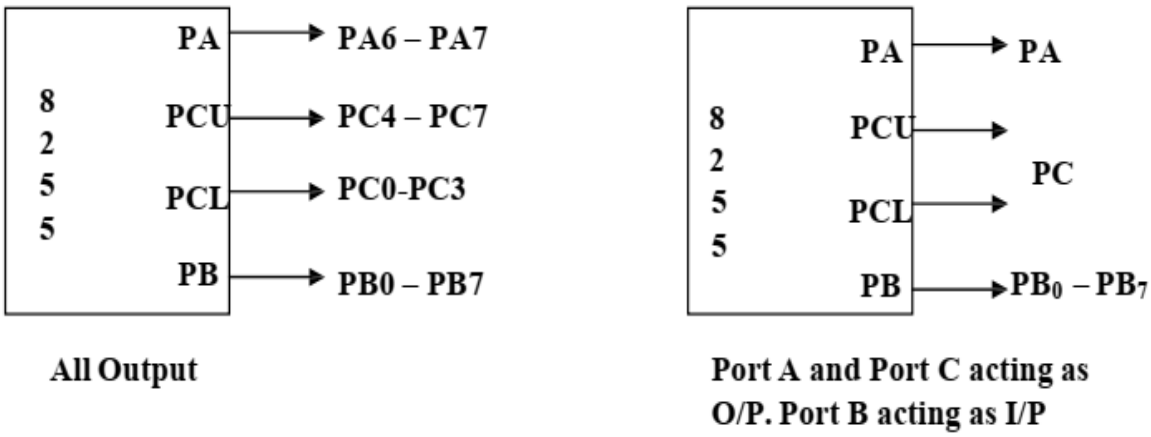
# Modes of Operation of 8255

- These are two basic modes of operation of 8255. I/O mode and Bit Set-Reset mode (BSR).
- In I/O mode, the 8255 ports work as programmable I/O ports, while in BSR mode only port C (PC0-PC7) can be used to set or reset its individual port bits.
- Under the I/O mode of operation, further there are three modes of operation of 8255, so as to support different types of applications, mode 0, mode 1 and mode 2.
- ***BSR Mode***: In this mode any of the 8-bits of port C can be set or reset depending on D0 of the control word. The bit to be set or reset is selected by bit select flags D3, D2 and D1 of the CWR as given in table.
- **I/O Modes** :

**a)** ***Mode 0 (Basic I/O mode):*** This mode is also called as basic input/output mode. This mode provides simple input and output capabilities using each of the three ports. Data can be simply read from and written to the input and output ports respectively, after appropriate initialization.

| $D_3$ | $D_2$ | $D_1$ | Selected bits of port C |
|---|---|---|---|
| 0 | 0 | 0 | $D_0$ |
| 0 | 0 | 1 | $D_1$ |
| 0 | 1 | 0 | $D_2$ |
| 0 | 1 | 1 | $D_3$ |
| 1 | 0 | 0 | $D_4$ |
| 1 | 0 | 1 | $D_5$ |
| 1 | 1 | 0 | $D_6$ |
| 1 | 1 | 1 | $D_7$ |

## BSR Mode : CWR Format

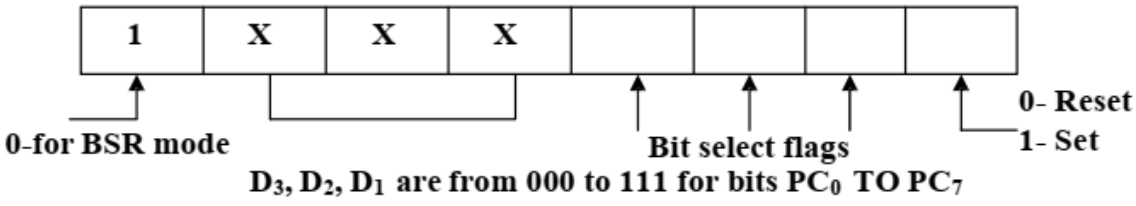



# Mode 0

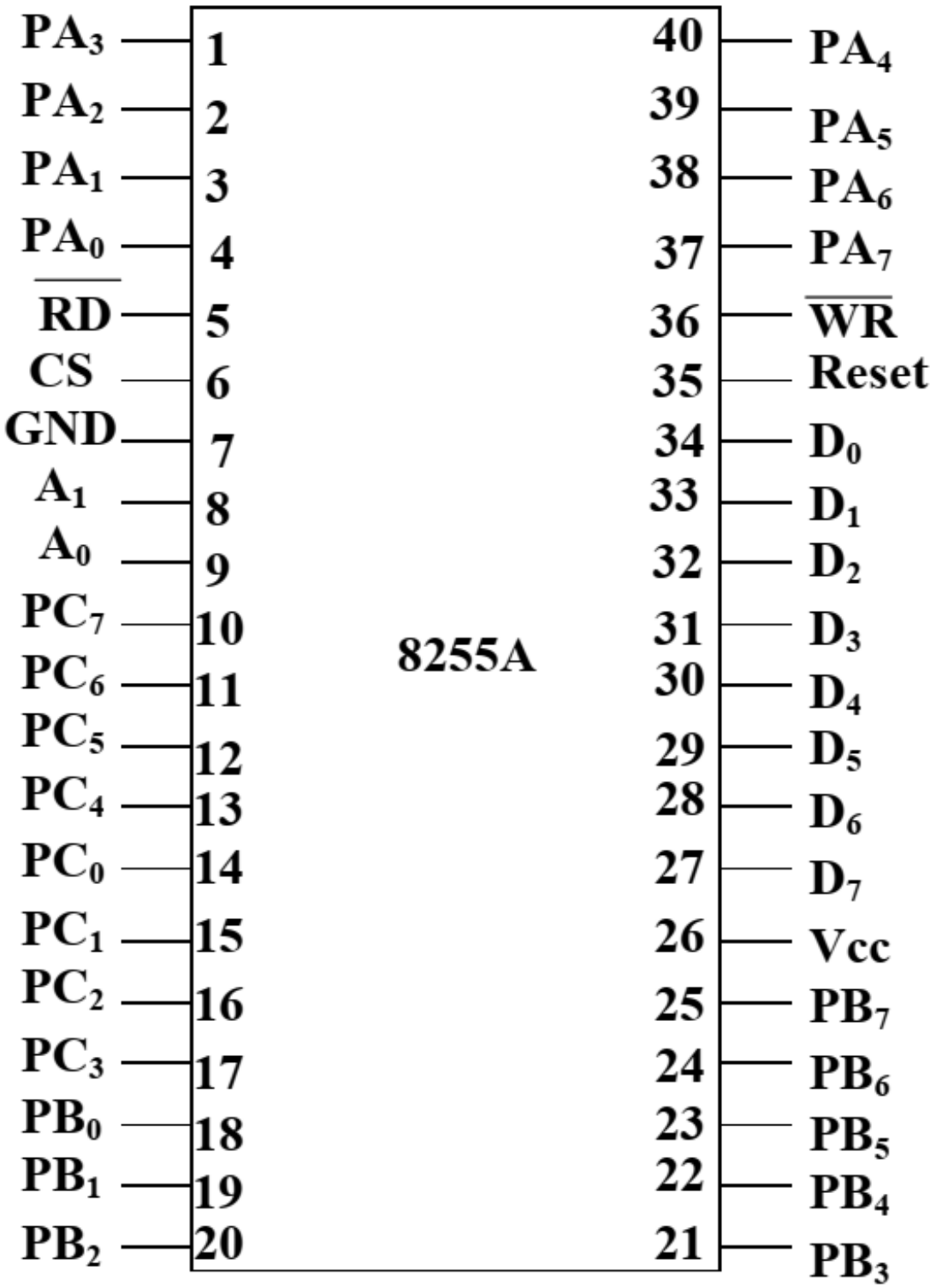
- The salient features of this mode are as listed below:

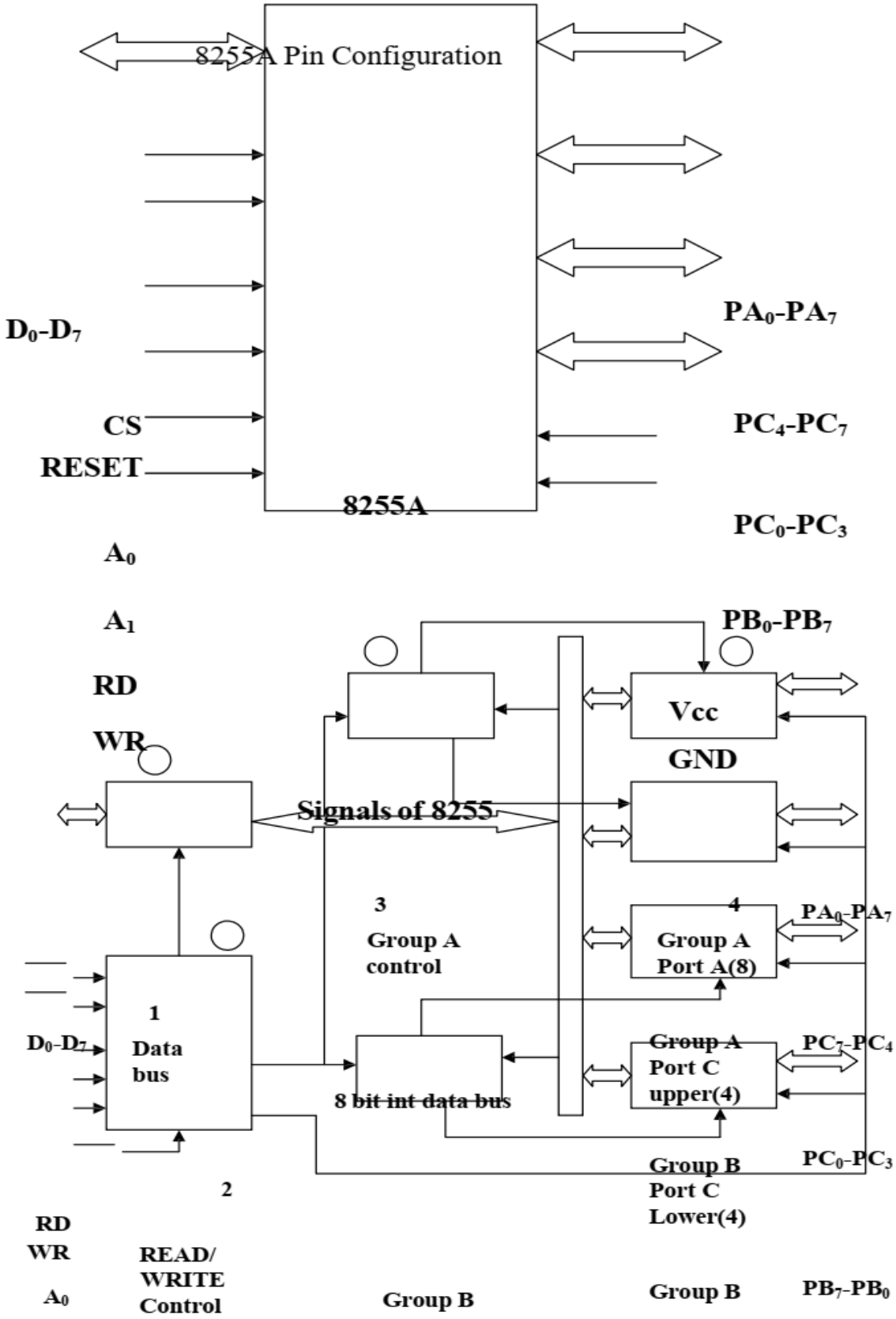
1. Two 8-bit ports (port A and port B)and two 4-bit ports (port C upper and lower)are available. The two 4-bit ports can be combinedly used as a third 8-bit port.
2. Any port can be used as an input or output port.
3. Output ports are latched. Input ports are not latched.
4. A maximum of four ports are available so that overall 16 I/O configuration are possible.

- All these modes can be selected by programming a register internal to 8255 known as CWR.
- The control word register has two formats. The first format is valid for I/O modes of operation, i.e. modes 0, mode 1 and mode 2 while the second format is valid for bit set/reset (BSR) mode of operation. These formats are shown in following fig.



**I/O Mode Control Word Register Format and**
**BSR Mode Control Word Register Format**




8255A Pin Configuration
D0-D7
CS
RESET
A0
A1
RD
WR
8255A
PA0-PA7
PC4-PC7
PC0-PC3
PB0-PB7
Vcc
GND
Signals of 8255
3
Group A
control
4
Group A
Port A(8)
PA0-PA7
1
Data
bus
D0-D7
8 bit int data bus
Group A
Port C
upper(4)
PC7-PC4
Group B
Port C
Lower(4)
PC0-PC3
2
RD
WR
A0
READ/
WRITE
Control
Group B
Group B
PB7-PB0

$A_1$

**RESET**

**CS**